Click here for production status of specific part numbers.

MAX9723

Stereo DirectDrive Headphone Amplifier with BassMax, Volume Control, and I²C

General Description

The MAX9723 stereo DirectDrive® headphone amplifier with BassMax and volume control is ideal for portable audio applications where space is at a premium and performance is essential. The MAX9723 operates from a single 1.8V to 3.6V power supply and includes features that reduce external component count, system cost, board space, and improves audio reproduction.

The headphone amplifier uses Maxim's DirectDrive architecture that produces a ground-referenced output from a single supply, eliminating the need for large DC-blocking capacitors. The headphone amplifiers deliver 62mW into a 16Ω load, feature low 0.006% THD+N, and high 90dB PSRR. The MAX9723 features Maxim's industry-leading click-and-pop suppression.

The BassMax feature boosts the bass response of the amplifier, improving audio reproduction when using inexpensive headphones. The integrated volume control features 32 discrete volume levels, eliminating the need for an external potentiometer. BassMax and the volume control are enabled through the I²C/SMBus™-compatible interface. Shutdown is controlled through either the hardware or software interfaces.

The MAX9723 consumes only 3.7mA of supply current at 1.8V, provides short-circuit and thermal-overload protection, and is fully specified over the extended -40°C to +85°C temperature range. The MAX9723 is available in a tiny (2mm x 2mm x 0.62mm) 16-bump chip-scale package (UCSP™) or 16-pin thin QFN (4mm x 4mm x 0.8mm) package.

Applications

- PDA Audio
- Portable CD Players
- Mini Disc Players
- MP3-Enabled Cellular
- Phones
- MP3 Players

Selector Guide

PART	SLAVE ADDRESS	MAXIMUM GAIN (dB)
MAX9723A	1001100	0
MAX9723B	1001101	0
MAX9723C	1001100	+6
MAX9723D	1001101	+6

DirectDrive is a registered trademark of Maxim Integrated Products, Inc.
SMBus is a trademark of Intel Corp.
UCSP is a trademark of Maxim Integrated Products, Inc.

Features

- 62mW, DirectDrive Headphone Amplifier Eliminates Bulky DC-Blocking Capacitors
- 1.8V to 3.6V Single-Supply Operation
- Integrated 32-Level Volume Control
- High 90dB PSRR at 1kHz
- Low 0.006% THD+N
- Industry-Leading Click-and-Pop Suppression
- ±8kV HBM ESD-Protected Headphone Outputs
- Short-Circuit and Thermal-Overload Protection
- Low-Power Shutdown Mode (5µA)
- Software-Enabled Bass Boost (BassMax)
- I²C/SMBus-Compatible Interface
- Available in Space-Saving, Thermally Efficient Packages:
  - 16-Bump UCSP (2mm x 2mm x 0.62mm)
  - 16-Pin Thin QFN (4mm x 4mm x 0.8mm)

Ordering Information

PART**	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX9723_EBE-T*	-40°C to +85°C	16 UCSP-16	B16-1
MAX9723_ETE+	-40°C to +85°C	16 TQFN	T1644-4

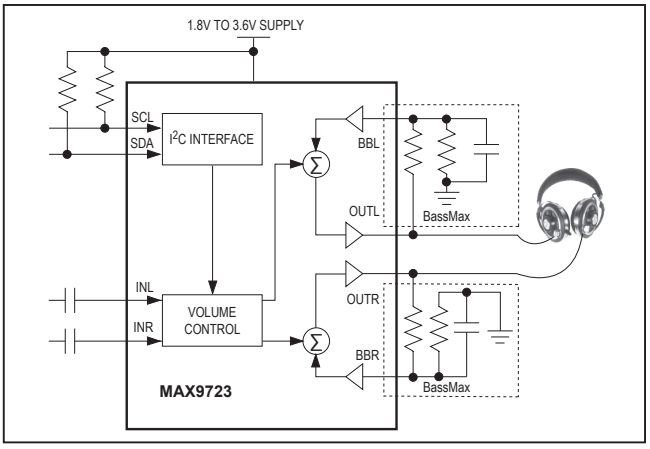
***Replace the '_' with the one-letter code that denotes the slave address and maximum programmable gain. See the Selector Guide.*

+Denotes a lead-free/RoHS-compliant package.

**Future product—contact factory for availability.*

Pin Configurations appears at end of data sheet.

Block Diagram



maxim integrated™

Absolute Maximum Ratings

SGND to PGND .....-0.3V to +0.3V
V_{DD} to PGND.....-0.3V to +4V
PV_{SS} to SV_{SS}.....-0.3V to +0.3V
C1P to PGND.....-0.3V to (V_{DD} + 0.3V)
C1N to PGND.....(PV_{SS} - 0.3V) to +0.3V
PV_{SS}, SV_{SS} to PGND.....+0.3V to -4V
IN_ to SGND.....(SV_{SS} - 0.3V) to (V_{DD} + 0.3V)
SDA, SCL to PGND.....-0.3V to +4V
$\overline{SHDN}$ to PGND.....-0.3V to (V_{DD} + 0.3V)
OUT_ to SGND.....-3V to +3V
BB_ to SGND.....-2V to +2V
Duration of OUT_ Short Circuit to _GND .....Continuous

Continuous Current Into/Out of:
V_{DD}, C1P, PGND, C1N, PV_{SS}, SV_{SS}, or OUT_.....±0.85A
Any Other Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
4 x 4 UCSP (derate 8.2mW/°C above +70°C).....659.2mW
16-Pin Thin QFN (derate 16.9mW/°C above +70°C)....1349mW
Operating Temperature Range.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering)
Reflow .....+230°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DD} = $\overline{SHDN}$ = 3V, PGND = SGND = 0V, C1 = C2 = 1µF, BB_ = 0V. gain = 0dB, maximum volume, BassMax disabled. Load connected between OUT_ and SGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL							
Supply Voltage Range	V_{DD}			1.8		3.6	V
Quiescent Supply Current	I_{DD}	No load			4	6.5	mA
Shutdown Supply Current	I_{DD_SHDN}	$V_{\overline{SHDN}}$ = 0V			5	8.5	µA
Turn-On Time	t_{ON}				200		µs
Turn-Off Time	t_{OFF}				35		µs
Thermal Shutdown Threshold	T_{THRES}				+143		°C
Thermal Shutdown Hysteresis	T_{HYST}				12		°C
HEADPHONE AMPLIFIER							
Output Offset Voltage	V_{OS}	Measured between OUT_ and SGND (Note 2)	Gain = 0dB, MAX9723A/ MAX9723B		±0.7	±4.5	mV
			Gain = +6dB, MAX9723C/ MAX9723D		±0.8	±5	
Input Resistance	R_{IN}	All volume levels		10	17	27	kΩ
BBR, BBL Input Bias Current	I_{BIAS_BB}				±10	±100	nA
Power-Supply Rejection Ratio	PSRR	(Note 2)	DC, V_{DD} = 1.8V to 3.6V	73	90		dB
			f = 217Hz, 100mV_{P-P} ripple, V_{DD} = 3.0V		87		
			f = 1kHz, 100mV_{P-P} ripple, V_{DD} = 3.0V		86		
			f = 20kHz, 100mV_{P-P} ripple, V_{DD} = 3.0V		61		

Electrical Characteristics (continued)

(V_{DD} = $\overline{SHDN}$ = 3V, PGND = SGND = 0V, C1 = C2 = 1µF, BB_ = 0V. gain = 0dB, maximum volume, BassMax disabled. Load connected between OUT_ and SGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Power	P_{OUT}	THD+N = 1%, f_{IN} = 1kHz	R_L = 32Ω			59		mW
			R_L = 16Ω (Note 5)		38	60		
Total Harmonic Distortion Plus Noise	THD+N	R_L = 16Ω, P_{OUT} = 35mW, f_{IN} = 1kHz				0.006		%
		R_L = 32Ω, P_{OUT} = 45mW, f_{IN} = 1kHz				0.004		
Maximum Gain	A_{MAX}	MAX9723A/ MAX9723B	Gain range bit 5 = 1			0		dB
			Gain range bit 5 = 0			-5		
		MAX9723C/ MAX9723D	Gain range bit 5 = 1			+6		dB
			Gain range bit 5 = 0			+1		
Signal-to-Noise Ratio	SNR	R_L = 32Ω, V_{OUT} = 1V_{RMS}	BW = 22Hz to 22kHz			99		dB
			A-weighted			100		
Slew Rate	SR					0.35		V/µs
Capacitive Drive		No sustained oscillations				300		pF
Output Resistance in Shutdown	R_{OUT_SHDN}	$V_{\overline{SHDN}}$ = 0V, measured from OUT_ to SGND				20		kΩ
Output Capacitance in Shutdown	C_{OUT_SHDN}	$V_{\overline{SHDN}}$ = 0V, measured from OUT_ to SGND				60		pF
Click/Pop Level	K_{CP}	R_L = 32Ω, peak voltage, A-weighted, 32 samples per second (Notes 2, 4)	MAX9723A/ MAX9723B	Into shutdown		-69		dB
				Out of shutdown		-71		
			MAX9723C/ MAX9723D	Into shutdown		-70		
				Out of shutdown		-69		
Charge-Pump Switching Frequency	f_{CP}				505	600	700	kHz
Crosstalk	XTALK	L to ≥ or ≥ to L, f = 10kHz, V_{OUT} = 1V_{P-P}, R_L = 32Ω, both channels loaded				80		dB
DIGITAL INPUTS ($\overline{SHDN}$, SDA, SCL)								
Input High Voltage	V_{IH}				0.7 x V_{DD}			V
Input Low Voltage	V_{IL}						0.3 x V_{DD}	V
Input Leakage Current							P1	µA
DIGITAL OUTPUTS (SDA)								
Output Low Voltage	V_{OL}	I_{OL} = 3mA					0.4	V
Output High Current	I_{OH}	V_{SDA} = V_{DD}					1	µA

Timing Characteristics

(V_{DD} = $\overline{SHDN}$ = 3V, PGND = SGND = 0V, C1 = C2 = 1µF, BB_ = 0V. gain = 0dB, maximum volume, BassMax disabled. Load connected between OUT_ and SGND where specified. T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C, see Timing Diagram.) (Notes 1, 3)

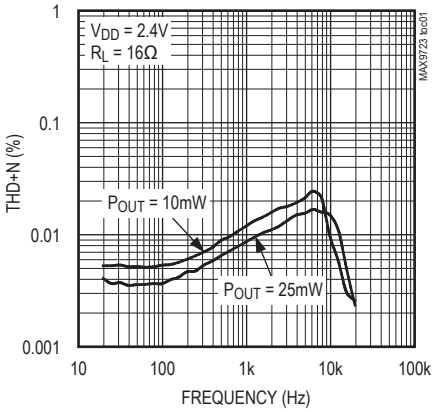
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Maximum Rise Time of SDA and SCL Signals	t_r			300		ns
Maximum Fall Time of SDA and SCL Signals	t_f			300		ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Pulse Width of Suppressed Spike	t_{SP}			100		ns
Maximum Capacitive Load for Each Bus Line	C_{L_BUS}			400		pF

Note 1: All specifications are 100% tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 2: Inputs AC-coupled to SGND.
Note 3: Guaranteed by design.
Note 4: Headphone mode testing performed with a 32Ω resistive load connected to GND. Mode transitions are controlled by $\overline{SHDN}$. The KCP level is calculated as: 20 x log [(level peak voltage during mode transition, no input signal)/(peak voltage under normal operation at rated power)]. Units are expressed in dB.
Note 5: Output power MIN is specified at T_A = +25°C.

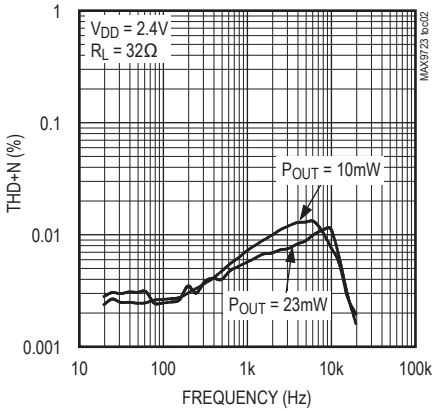
Typical Operating Characteristics

(V_{DD} = $\overline{SHDN}$ = 3V, PGND = SGND = 0V, C1 = C2 = 1µF, BB_ = 0V, gain = 0dB, maximum volume, BassMax disabled. Load connected between OUT_ and SGND where specified. Outputs in phase, both channels loaded. T_A = +25°C, unless otherwise noted.) (*See Functional Diagram/Typical Operating Circuit*)

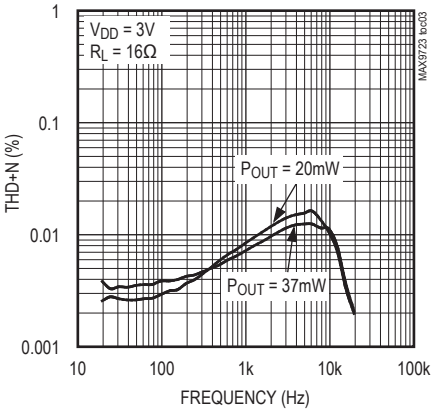
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



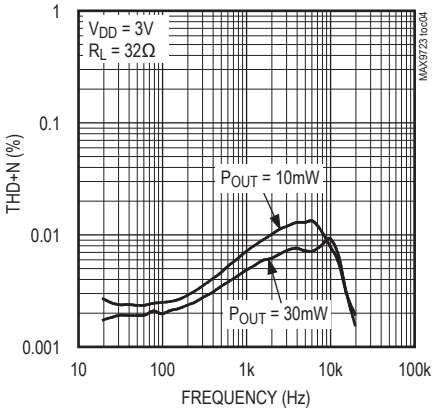
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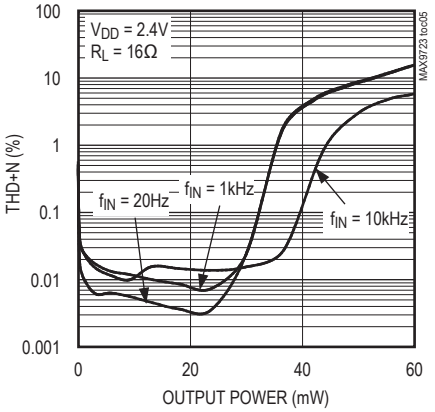
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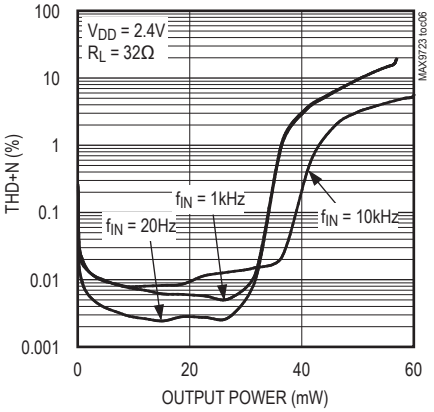
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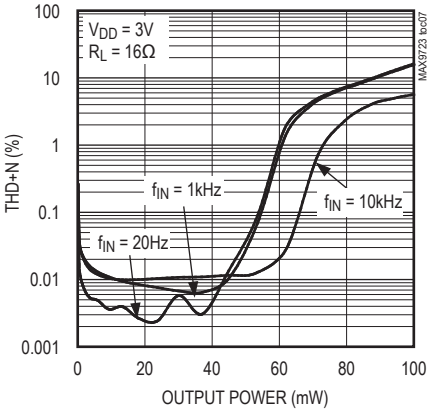
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



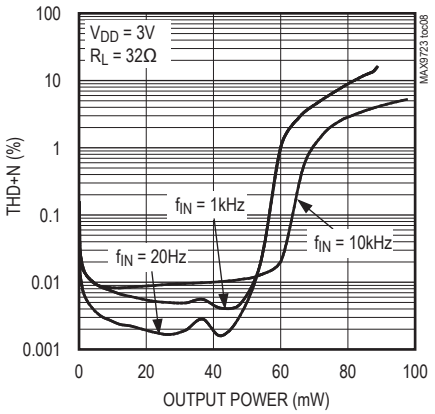
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



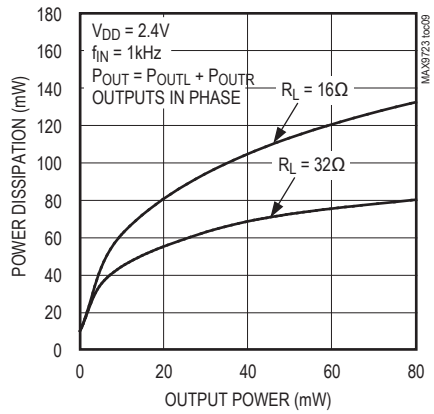
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



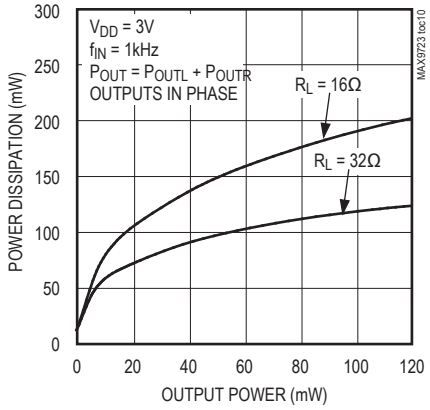
POWER DISSIPATION vs. OUTPUT POWER



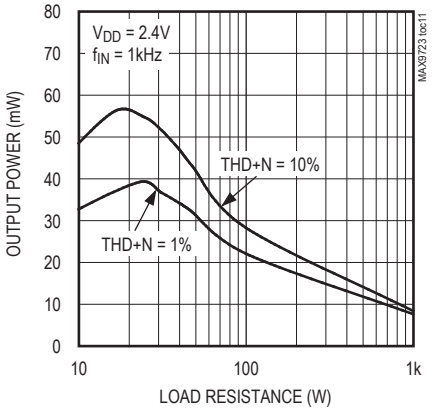
Typical Operating Characteristics (continued)

(V_{DD} = $\overline{SHDN}$ = 3V, PGND = SGND = 0V, C1 = C2 = 1µF, BB_ = 0V, gain = 0dB, maximum volume, BassMax disabled. Load connected between OUT_ and SGND where specified. Outputs in phase, both channels loaded. T_A = +25°C, unless otherwise noted.) (*See Functional Diagram/Typical Operating Circuit*)

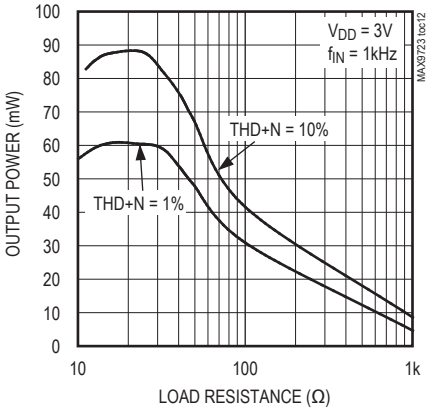
POWER DISSIPATION vs. OUTPUT POWER



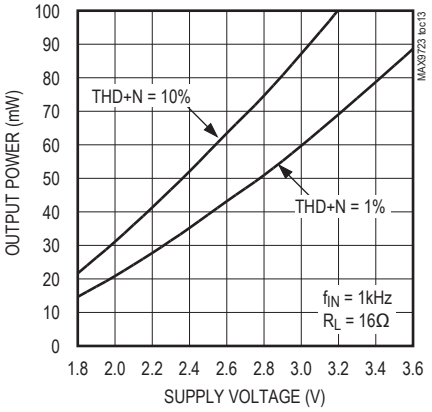
OUTPUT POWER vs. LOAD RESISTANCE



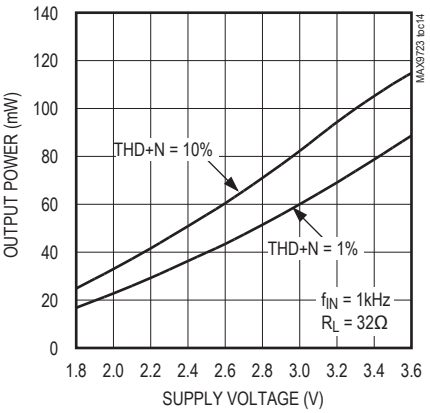
OUTPUT POWER vs. LOAD RESISTANCE



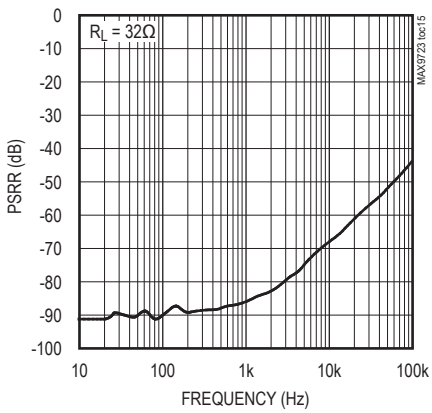
OUTPUT POWER vs. SUPPLY VOLTAGE



OUTPUT POWER vs. SUPPLY VOLTAGE



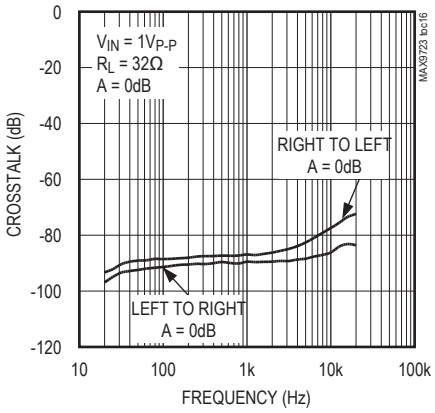
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



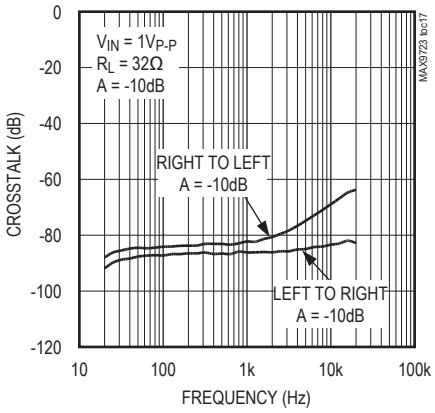
Typical Operating Characteristics (continued)

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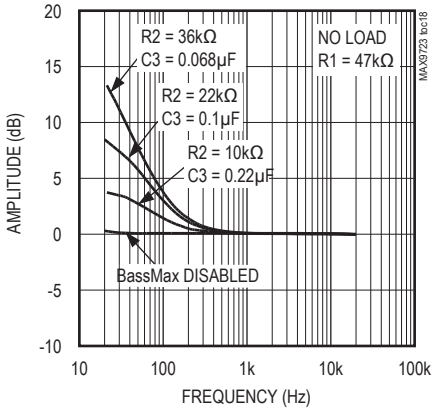
CROSSTALK vs. FREQUENCY



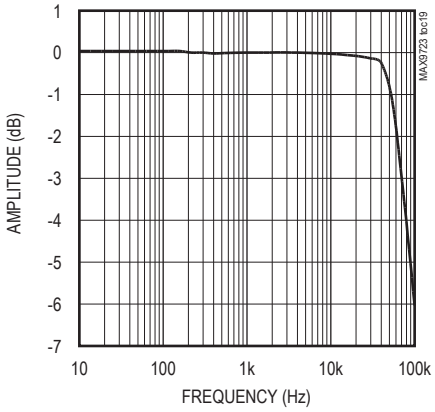
CROSSTALK vs. FREQUENCY



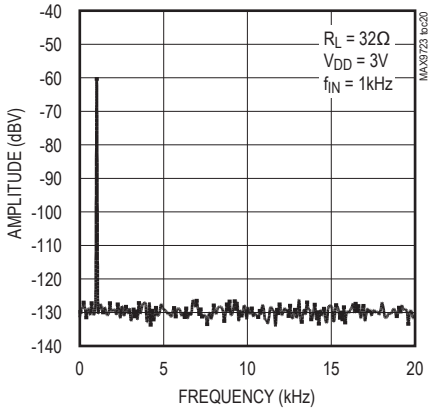
BASS BOOST FREQUENCY RESPONSE



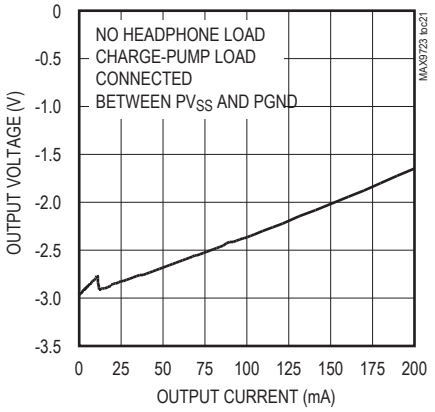
GAIN FLATNESS vs. FREQUENCY



OUTPUT SPECTRUM vs. FREQUENCY



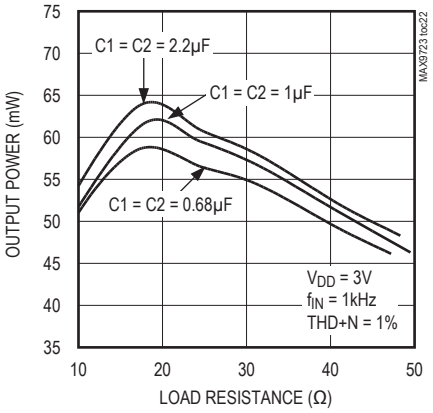
CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT



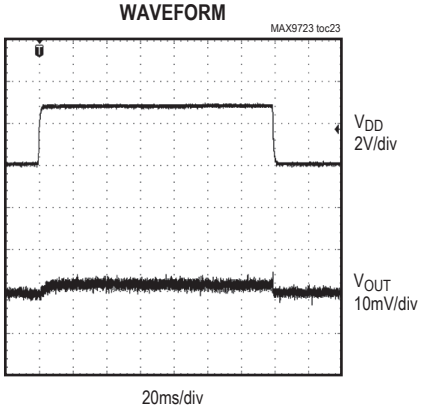
Typical Operating Characteristics (continued)

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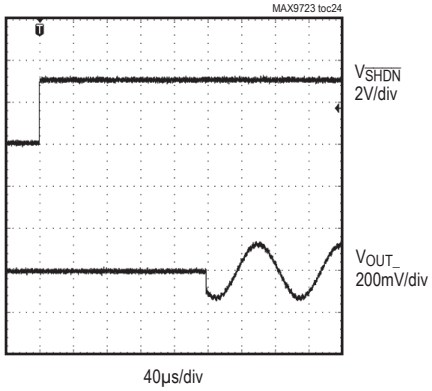
OUTPUT POWER vs. CHARGE-PUMP CAPACITANCE AND LOAD RESISTANCE



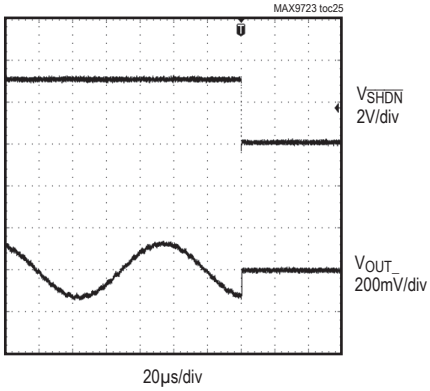
POWER-UP/POWER-DOWN WAVEFORM



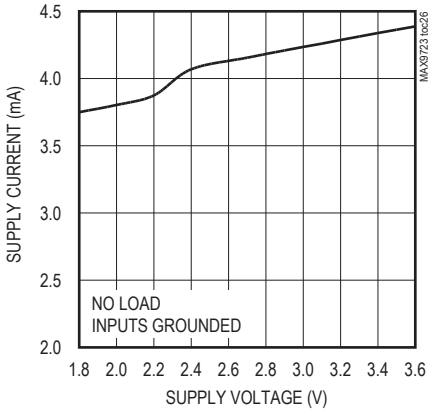
EXITING SHUTDOWN



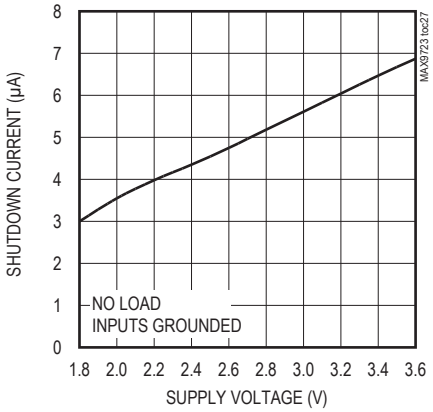
ENTERING SHUTDOWN



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN	BUMP	NAME	FUNCTION
THIN QFN	UCSP		
1	D1	V_{DD}	Power-Supply Input. Bypass V_{DD} to PGND with a 1µF capacitor.
2	C1	C1P	Charge-Pump Flying Capacitor Positive Terminal
3	B1	PGND	Power Ground. Connect to SGND.
4	A1	C1N	Charge-Pump Flying Capacitor Negative Terminal
5	B2	SCL	Serial Clock Input. Connect a 10kI pullup resistor from SCL to V_{DD}.
6	A2	PV_{SS}	Charge-Pump Output. Connect to SV_{SS}. Bypass PV_{SS} with a 1µF capacitor to PGND.
7	A3	SDA	Serial-Data Input. Connect a 10kΩ pullup resistor from SDA to V_{DD}.
8	B3	$\overline{SHDN}$	Shutdown. Drive $\overline{SHDN}$ low to disable the MAX9723. Connect $\overline{SHDN}$ to V_{DD} while bit 7 is high for normal operation (see the *Command Register* section).
9	A4	SGND	Signal Ground. Connect to PGND.
10	B4	INL	Left-Channel Input
11	C4	INR	Right-Channel Input
12	D4	SV_{SS}	Headphone Amplifier Negative Power-Supply Input. Connect to PV_{SS}.
13	C3	BBR	Right BassMax Input. Connect an external lowpass filter between OUTR and BBR to apply bass boost to the right-channel output. Connect BBR to SGND if BassMax is not used (see the *BassMax (Bass Boost)* section).
14	D3	OUTR	Right Headphone Output
15	D2	OUTL	Left Headphone Output
16	C2	BBL	Left BassMax Input. Connect an external lowpass filter between OUTL and BBL to apply bass boost to the left-channel output. Connect BBL to SGND if BassMax is not used (see the *BassMax (Bass Boost)* section).
EP	—	EP	Exposed Paddle. Connect EP to SV_{SS} or leave unconnected.

Detailed Description

The MAX9723 stereo headphone amplifier features Maxim's DirectDrive architecture, eliminating the large output-coupling capacitors required by conventional single-supply headphone amplifiers. The MAX9723 consists of two 62mW Class AB headphone amplifiers, hardware/software shutdown control, inverting charge pump, integrated 32-level volume control, BassMax circuitry, comprehensive click-and-pop suppression circuitry, and an I2C-compatible interface (see the *Functional Diagram/Typical Operating Circuit*). A negative power supply (PV_{SS}) is created internally by inverting the positive supply (V_{DD}). Powering the amplifiers from V_{DD} and PV_{SS} increases the dynamic range of the amplifiers to almost twice that of other single-supply amplifiers, increasing the total available output power.

The MAX9723 DirectDrive outputs are biased at SGND (see Figure 1). The benefit of this 0V bias is that the amplifier outputs do not have a DC component, eliminating the need for large DC-blocking capacitors. Eliminating the DC-blocking capacitors on the output saves board space, system cost, and improves low-frequency response.

An I2C-compatible interface allows serial communication between the MAX9723 and a microcontroller. The MAX9723 is available with two different I2C addresses allowing two MAX9723 ICs to share the same bus (see Table 1). The internal command register controls the shutdown status of the MAX9723, enables the BassMax circuitry, sets the maximum gain of the amplifier, and sets the volume level (see Table 2). The MAX9723's BassMax circuitry improves audio reproduction by boosting the bass response of the amplifier, compensating for any low-frequency attenuation introduced by the headphone. The

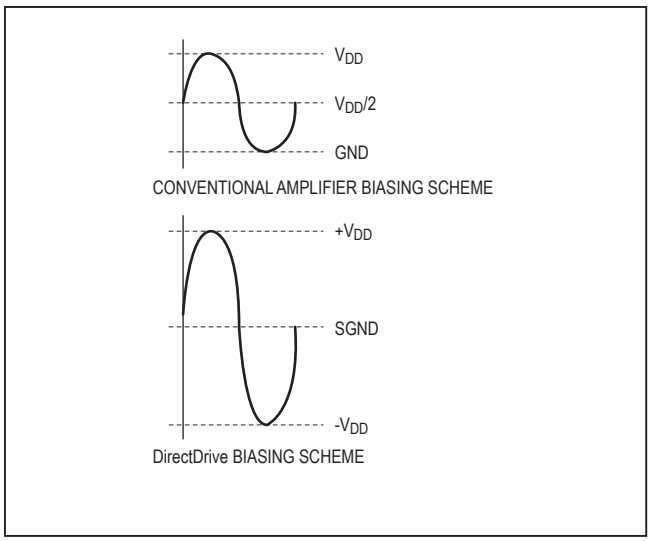


Figure 1. Traditional Amplifier Output vs. MAX9723 DirectDrive Output

MAX9723A and MAX9723B have a maximum amplifier gain of 0dB while the MAX9723C and MAX9723D have a maximum gain of +6dB. Amplifier volume is digitally programmable to any one of 32 levels.

DirectDrive

Traditional single-supply headphone amplifiers have their outputs biased at a nominal DC voltage, typically half the supply, for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both headphone and headphone amplifier.

Maxim's DirectDrive architecture uses a charge pump to create an internal negative supply voltage. This allows the MAX9723 headphone amplifier outputs to be biased at 0V, almost doubling the dynamic range while operating from a single supply. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (typically 220µF) tantalum capacitors, the MAX9723 charge pump requires only two small 1µF ceramic capacitors, thereby conserving board space, reducing cost, and improving the low-frequency response of the headphone amplifier. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics* for details of the possible capacitor sizes.

In addition to the cost and size disadvantages, the DC-blocking capacitors required by conventional headphone amplifiers limit low-frequency response and can distort the audio signal.

Previous attempts at eliminating the output-coupling capacitors involved biasing the headphone return (sleeve) to the DC bias voltage of the headphone amplifiers. This method raises some issues:

1) The sleeve is typically grounded to the chassis. Using the midrail biasing approach, the sleeve must be isolated from system ground, complicating product design. The DirectDrive output biasing scheme allows the sleeve to be grounded.
2) During an ESD strike, the amplifier's ESD structure is the only path to system ground. The amplifier must be able to withstand the full ESD strike. The MAX9723 headphone outputs can withstand an ±8kV ESD strike (HBM).
3) When using the headphone jack as a line out to other equipment, the bias voltage on the sleeve may conflict with the ground potential from other equipment, resulting in possible damage to the amplifiers. The DirectDrive outputs of the MAX9723 can be directly coupled to other ground-biased equipment.

Charge Pump

The MAX9723 features a low-noise charge pump. The 600kHz switching frequency is well beyond the audio range, and does not interfere with the audio signals. This enables the MAX9723 to achieve a 99dB SNR. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Limiting the switching speed of the charge pump minimizes di/dt noise caused by the parasitic bond wire and trace inductance. Although not typically required, additional high-frequency noise attenuation can be achieved by increasing the size of C2 (see the *Functional Diagram/Typical Operating Circuit*).

Shutdown

The MAX9723 features a 5µA, low-power shutdown mode that reduces quiescent current consumption and extends battery life. Shutdown is controlled by a hardware or software interface. Driving $\overline{SHDN}$ low disables the drive amplifiers, bias circuitry, charge pump, and sets the headphone amplifier output impedance to 20kΩ. Similarly, the MAX9723 enters shutdown when bit seven (B7) in the control register is reset. $\overline{SHDN}$ and B7 must be high to enable the MAX9723. The I2C interface is active and the contents of the command register are not affected when in shutdown. This allows the master to write to the MAX9723 while in shutdown.

Click-and-Pop Suppression

The output-coupling capacitor is a major contributor of audible clicks and pops in conventional single-supply headphone amplifiers. The amplifier charges the coupling capacitor to its output bias voltage at startup. During shutdown the capacitor is discharged. This charging and discharging results in a DC shift across the capacitor, which appears as an audible transient at the speaker. Since the MAX9723 headphone amplifier does not require output-coupling capacitors, no audible transients occur.

Additionally, the MAX9723 features extensive click-and-pop suppression that eliminates any audible transient sources internal to the device. The Power-Up/Power-Down Waveform in the *Typical Operating Characteristics* shows that there are minimal transients at the output upon startup or shutdown.

In most applications, the preamplifier driving the MAX9723 has a DC bias of typically half the supply. The input-coupling capacitor is charged to the preamplifier's bias voltage through the MAX9723's input impedance (R_{IN}) during start-up. The resulting voltage shift across the capacitor creates an audible click/pop. To avoid clicks/pops caused by the input filter, delay the rise of $\overline{SHDN}$ by at least 4 time constants, 4 x R_{IN} x C_{IN}, relative to the start of the preamplifier.

BassMax (Bass Boost)

Typical headphones do not have a flat-frequency response. The small physical size of the diaphragm does not allow the headphone speaker to efficiently reproduce low frequencies. This physical limitation results in attenuated bass response. The MAX9723 includes a bass boost feature that compensates for the headphone's poor bass response by increasing the amplifier gain at low frequencies.

The DirectDrive output of the MAX9723 has more headroom than typical single-supply headphone amplifiers. This additional headroom allows boosting the bass frequencies without the output-signal clipping.

Program the BassMax gain and cutoff frequency with external components connected between OUT_ and BB_ (see the *Functional Diagram/Typical Operating Circuit*). Use the I2C-compatible interface to program the command register to enable/disable the BassMax circuit.

BB_ is connected to the noninverting input of the output amplifier when BassMax is enabled. BB_ is pulled to SGND when BassMax is disabled. The typical application of the BassMax circuit involves feeding a lowpass version of the output signal back to the amplifier. This is realized using positive feedback from OUT_ to BB_. Figure 2 shows the connections needed to implement BassMax.

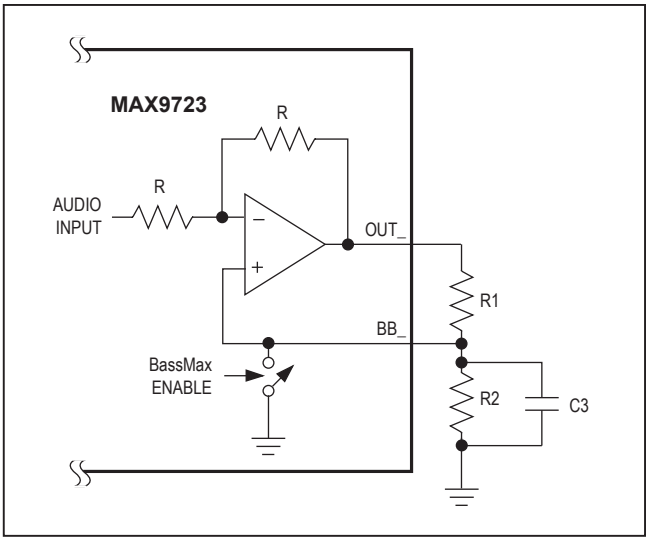


Figure 2. BassMax External Connections

Maximum Gain Control

The MAX9723A and MAX9723B have selectable maximum gains of -5dB or 0dB (see Table 5) while the MAX9723C and MAX9723D have selectable maximum gains of +1dB or +6dB (see Table 6). Bit 5 in the command register selects between the two maximum gain settings.

Volume Control

The MAX9723 includes a 32-level volume control that adjusts the gain of the output amplifiers according to the code contained in the command register. Volume is programmed through the command register bits [4:0]. Tables 7–10 show all of the available gain settings for the MAX9723A–MAX9723D. The mute attenuation is typically better than 100dB when driving a 32Ω load.

Serial Interface

The MAX9723 features an I2C/SMBus-compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX9723 and the master at clock rates up to 400kHz. Figure 3 shows the 2-wire interface timing diagram. The MAX9723 is a receive-only slave device relying on the master to generate the SCL signal. The MAX9723 cannot write to the SDA bus except to acknowledge the receipt of data from the master. The

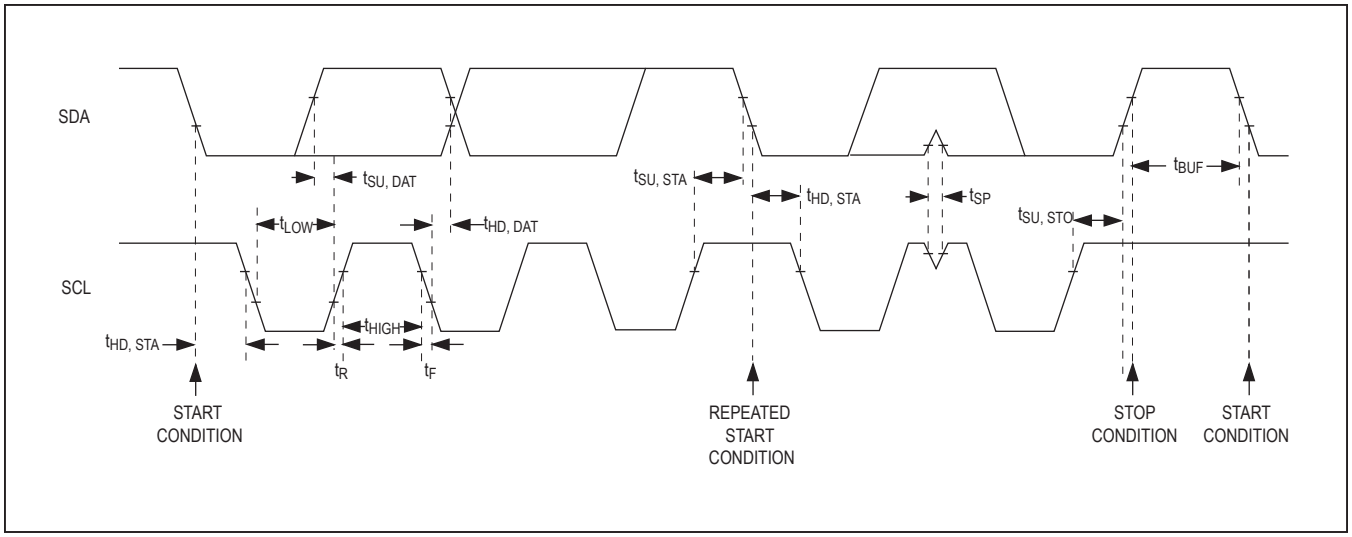


Figure 3. 2-Wire Serial-Interface Timing Diagram

master, typically a microcontroller, generates SCL and initiates data transfer on the bus.

A master device communicates to the MAX9723 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX9723 SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The MAX9723 SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9723 from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions section*). SDA and SCL idle high when the I2C bus is not busy.

Start and Stop Conditions

SDA and SCL idle high when the bus is not in use. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of transmission to the MAX9723. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

Early STOP Conditions

The MAX9723 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Slave Address

The MAX9723 is available with one of two preset slave addresses (see Table 1). The address is defined as the seven most significant bits (MSBs) followed by the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit. The address is the first byte of information sent to the MAX9723 after the START condition. The MAX9723 is a slave device only capable of being written to. The sent R/$\overline{\text{W}}$ bit must always be a zero when configuring the MAX9723.

The MAX9723 acknowledges the receipt of its address even if R/$\overline{\text{W}}$ is set to 1. However, the MAX9723 will not drive SDA. Addressing the MAX9723 with R/$\overline{\text{W}}$ set to 1 causes the master to receive all 1's regardless of the contents of the command register.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9723 uses to handshake receipt of each byte of

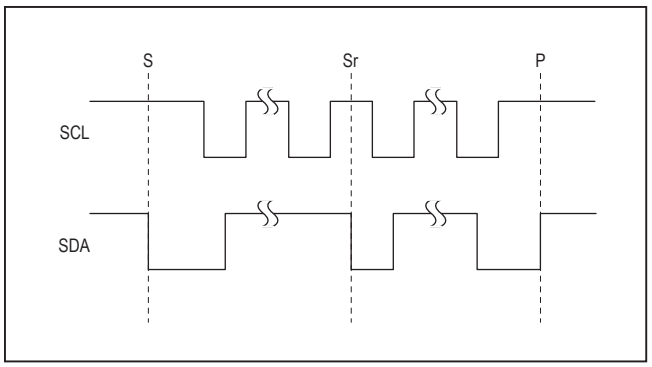


Figure 4. START, STOP, and REPEATED START Conditions

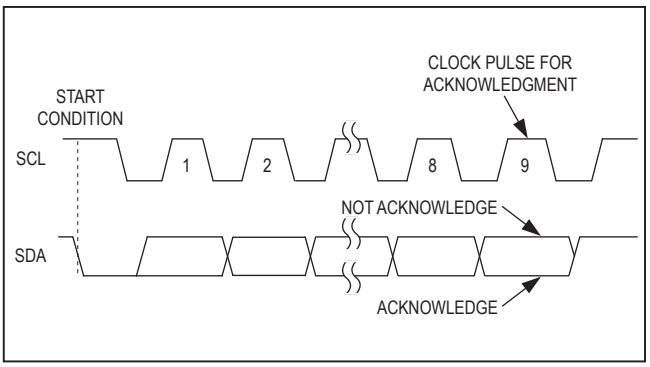


Figure 5. Acknowledge

Table 1. MAX9723 Address Map

PART	MAX9723 SLAVE ADDRESS							
	A6	A5	A4	A3	A2	A1	A0	R/$\overline{W}$
MAX9723A	1	0	0	1	1	0	0	0
MAX9723B	1	0	0	1	1	0	1	0
MAX9723C	1	0	0	1	1	0	0	0
MAX9723D	1	0	0	1	1	0	1	0

Table 2. MAX9723 Command Register

B7	B6	B5	B4	B3	B2	B1	B0
SHUTDOWN	BassMax ENABLE	MAXIMUM GAIN	VOLUME				

Table 3. Shutdown Control, $\overline{SHDN}$ = 1

MODE	B7
MAX9723 Disabled	0
MAX9723 Enabled	1

Table 4. BassMax Control

MODE	B6
BassMax Disabled	0
BassMax Enabled	1

data (see Figure 5). The MAX9723 pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master may reattempt communication.

Write Data Format

A write to the MAX9723 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit reset to 0 (see Table 1), one byte of data to configure the command register, and a STOP condition. Figure 6 illustrates the proper format for one frame.

The MAX9723 only accepts write data, but it acknowledges the receipt of its address byte with the R/$\overline{W}$ bit set high. The MAX9723 does not write to the SDA bus in the event that the R/W bit is set high. Subsequently, the master reads all 1's from the MAX9723. Always reset the R/$\overline{W}$ bit to 0 to avoid this situation.

Command Register

The MAX9723 has one command register that is used to enable/disable shutdown, enable/disable BassMax, and set the maximum gain and volume. Table 2 describes the function of the bits contained in the command register.

Reset B7 to 0 to shut down the MAX9723. The MAX9723 wakes up from shutdown when B7 is set to 1 provided $\overline{SHDN}$ is high. $\overline{SHDN}$ must be high and B7 must be set to 1 for the MAX9723 to operate normally (see Table 3).

Set B6 to 1 to enable BassMax (see Table 4). The output signal's low-frequency response will be boosted according to the external components connected between OUT_ and BB_. See the *BassMax Gain-Setting Components* section in the *Applications Information* section for details on choosing the external components.

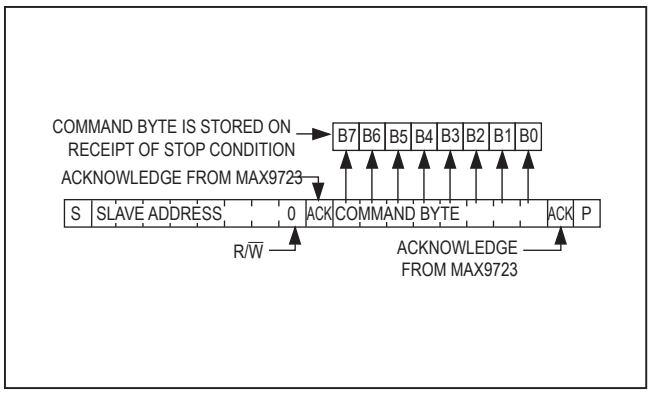


Figure 6. Write Data Format Example

The MAX9723A and MAX9723B have a maximum gain setting of -5dB or 0dB, while the MAX9723C and MAX9723D have a maximum gain setting of +1dB or +6dB. B5 in the command register programs the maximum gain (see Tables 5 and 6).

Adjust the MAX9723's amplifier gain with the volume control bits [4:0]. The gain is adjustable to one of 32 steps ranging from full mute to the maximum gain programmed by B5. Tables 7–10 list all the possible gain settings for the MAX9723. Figures 7–10 show the volume control transfer functions for the MAX9723.

Power-On Reset

The contents of the MAX9723's command register at power-on are shown in Table 11.

Applications Information

Power Dissipation and Heat Sinking

Linear power amplifiers can dissipate a significant amount of power under normal operating conditions. The maximum power dissipation for each package is given in the *Absolute Maximum Ratings* section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where $T_{J(MAX)}$ is +150°C, T_A is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section. For example, θ_{JA} for the thin QFN package is +59°C/W.

The MAX9723 has two power dissipation sources, the charge pump and the two output amplifiers. If the power dissipation exceeds the rated package dissipation, reduce V_{DD}, increase load impedance, decrease the ambient temperature, or add heatsinking. Large output, supply, and ground traces decrease θ_{JA}, allowing more heat to be transferred from the package to surrounding air.

Table 5. MAX9723A and MAX9723B Maximum Gain Control

MAXIMUM GAIN (dB)	B5
-5	0
0	1

Table 6. MAX9723C and MAX9723D Maximum Gain Control

MAXIMUM GAIN (dB)	B5
+1	0
+6	1

Output Dynamic Range

Dynamic range is the difference between the noise floor of the system and the output level at 1% THD+N. It is essential that a system's dynamic range be known before setting the maximum output gain. Output clipping will occur if the output signal is greater than the dynamic range of the system. The DirectDrive architecture of the MAX9723 has increased dynamic range compared to other single-supply amplifiers.

Use the THD+N vs. Output Power in the *Typical Operating Characteristics* to identify the system's dynamic range. Find the output power that causes 1% THD+N for a given load. This point will indicate what output power causes the output to begin to clip. Use the following equation to determine the peak output voltage that causes 1% THD+N for a given load.

$$V_{OUT_(P-P)} = 2\sqrt{2(P_{OUT_1\%} \times R_L)}$$

where $P_{OUT_1\%}$ is the output power that causes 1% THD+N, R_L is the load resistance, and $V_{OUT_(P-P)}$ is the peak output voltage. After $V_{OUT_(P-P)}$ is identified, determine the peak input voltage that can be amplified without clipping:

$$V_{IN_(P-P)} = \frac{V_{OUT_(P-P)}}{10^{\left(\frac{A_V}{20}\right)}}$$

where $V_{IN_(P-P)}$ is the largest peak voltage that can be amplified without clipping, and A_V is the voltage gain

Table 7. MAX9723A and MAX9723B Gain Settings (B5 = 1, Max Gain = 0dB)

B4	B3	B2	B1	B0 (LSB)	GAIN (dB)
1	1	1	1	1	0
1	1	1	1	0	-0.5
1	1	1	0	1	-1
1	1	1	0	0	-1.5
1	1	0	1	1	-2
1	1	0	1	0	-2.5
1	1	0	0	1	-3
1	1	0	0	0	-4
1	0	1	1	1	-5
1	0	1	1	0	-6
1	0	1	0	1	-7
1	0	1	0	0	-9
1	0	0	1	1	-11
1	0	0	1	0	-13
1	0	0	0	1	-15
1	0	0	0	0	-17
0	1	1	1	1	-19
0	1	1	1	0	-21
0	1	1	0	1	-23
0	1	1	0	0	-25
0	1	0	1	1	-27
0	1	0	1	0	-29
0	1	0	0	1	-31
0	1	0	0	0	-33
0	0	1	1	1	-35
0	0	1	1	0	-37
0	0	1	0	1	-39
0	0	1	0	0	-41
0	0	0	1	1	-43
0	0	0	1	0	-45
0	0	0	0	1	-47
0	0	0	0	0	MUTE

of the amplifier in dB determined by the maximum gain setting (Bit 5) or the combination of the maximum gain setting plus bass boost (see the *BassMax Gain-Setting Components* section).

Table 8. MAX9723A and MAX9723B Gain Settings (B5 = 0, Max Gain = -5dB)

B4	B3	B2	B1	B0 (LSB)	GAIN (dB)
1	1	1	1	1	-5
1	1	1	1	0	-6
1	1	1	0	1	-7
1	1	1	0	0	-9
1	1	0	1	1	-11
1	1	0	1	0	-13
1	1	0	0	1	-15
1	1	0	0	0	-17
1	0	1	1	1	-19
1	0	1	1	0	-21
1	0	1	0	1	-23
1	0	1	0	0	-25
1	0	0	1	1	-27
1	0	0	1	0	-29
1	0	0	0	1	-31
1	0	0	0	0	-33
0	1	1	1	1	-35
0	1	1	1	0	-37
0	1	1	0	1	-39
0	1	1	0	0	-41
0	1	0	1	1	-43
0	1	0	1	0	-45
0	1	0	0	1	-47
0	1	0	0	0	-50
0	0	1	1	1	-53
0	0	1	1	0	-56
0	0	1	0	1	-59
0	0	1	0	0	-62
0	0	0	1	1	-65
0	0	0	1	0	-68
0	0	0	0	1	-71
0	0	0	0	0	MUTE

Component Selection

Input-Coupling Capacitor

The AC-coupling capacitor (C_{IN}) and internal gain-setting resistor form a highpass filter that removes any DC bias from an input signal (see the *Functional Diagram/ Typical Operating Circuit*). C_{IN} allows the MAX9723 to bias the

Table 9. MAX9723C and MAX9723D Gain Settings (B5 = 1, Max Gain = +6dB)

B4	B3	B2	B1	B0 (LSB)	GAIN (dB)
1	1	1	1	1	6
1	1	1	1	0	5.5
1	1	1	0	1	5
1	1	1	0	0	4.5
1	1	0	1	1	4
1	1	0	1	0	3.5
1	1	0	0	1	3
1	1	0	0	0	2
1	0	1	1	1	1
1	0	1	1	0	0
1	0	1	0	1	-1
1	0	1	0	0	-3
1	0	0	1	1	-5
1	0	0	1	0	-7
1	0	0	0	1	-9
1	0	0	0	0	-11
0	1	1	1	1	-13
0	1	1	1	0	-15
0	1	1	0	1	-17
0	1	1	0	0	-19
0	1	0	1	1	-21
0	1	0	1	0	-23
0	1	0	0	1	-25
0	1	0	0	0	-27
0	0	1	1	1	-29
0	0	1	1	0	-31
0	0	1	0	1	-33
0	0	1	0	0	-35
0	0	0	1	1	-37
0	0	0	1	0	-39
0	0	0	0	1	-41
0	0	0	0	0	MUTE

signal to an optimum DC level. The -3dB point of the high-pass filter, assuming zero-source impedance, is given by:

$$f_{-3dB} = \frac{1}{2\pi \times R_{IN} \times C_{IN}}$$

Table 10. MAX9723C and MAX9723D Gain Settings (B5 = 0, Max Gain = +1dB)

B4	B3	B2	B1	B0 (LSB)	GAIN (dB)
1	1	1	1	1	1
1	1	1	1	0	0
1	1	1	0	1	-1
1	1	1	0	0	-3
1	1	0	1	1	-5
1	1	0	1	0	-7
1	1	0	0	1	-9
1	1	0	0	0	-11
1	0	1	1	1	-13
1	0	1	1	0	-15
1	0	1	0	1	-17
1	0	1	0	0	-19
1	0	0	1	1	-21
1	0	0	1	0	-23
1	0	0	0	1	-25
1	0	0	0	0	-27
0	1	1	1	1	-29
0	1	1	1	0	-31
0	1	1	0	1	-33
0	1	1	0	0	-35
0	1	0	1	1	-37
0	1	0	1	0	-39
0	1	0	0	1	-41
0	1	0	0	0	-44
0	0	1	1	1	-47
0	0	1	1	0	-50
0	0	1	0	1	-53
0	0	1	0	0	-56
0	0	0	1	1	-59
0	0	0	1	0	-62
0	0	0	0	1	-65
0	0	0	0	0	MUTE

Table 11. Initial Power-Up Command Register Status

MODE	B7	B6	B5	B4	B3	B2	B1	B0
Power-On Reset	1	1	1	1	1	1	1	1

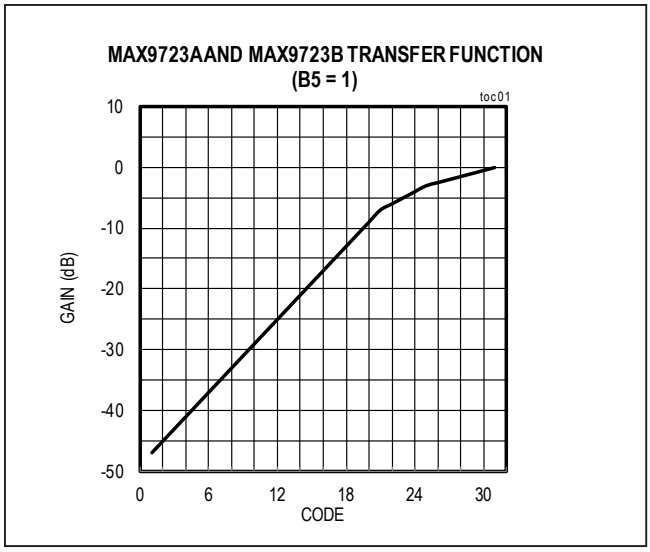


Figure 7. MAX9723A/MAX9723B Transfer Function with B5 = 1

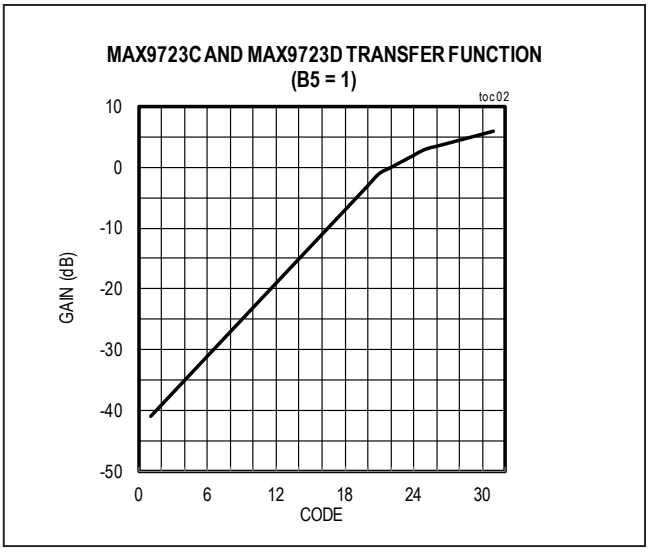


Figure 9. MAX9723C/MAX9723D Transfer Function with B5 = 1

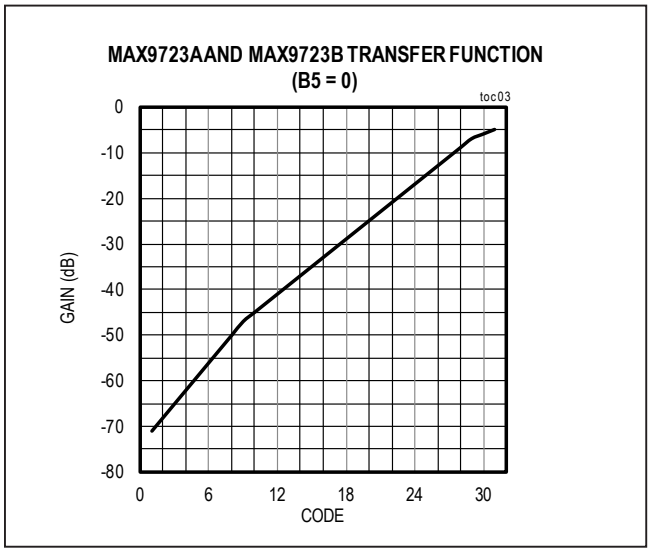


Figure 8. MAX9723A/MAX9723B Transfer Function with B5 = 0

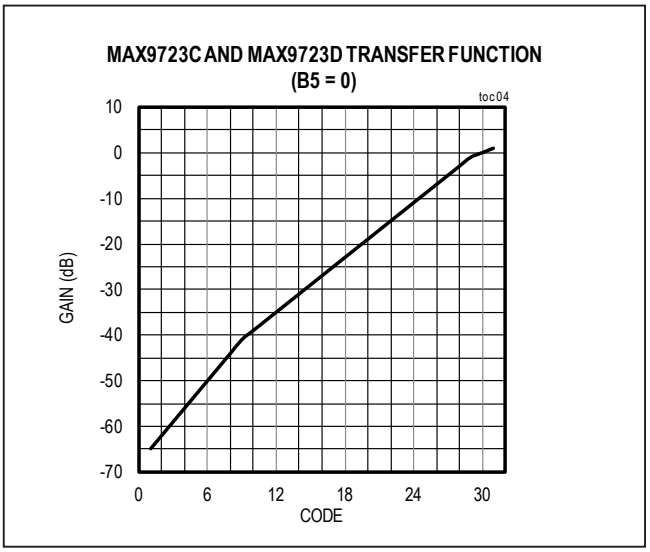


Figure 10. MAX9723C/MAX9723D Transfer Function with B5 = 0

where R_{IN} is a minimum of 10kΩ. Choose C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the amplifier's low-frequency response. Use capacitors with low-voltage coefficient dielectrics. Film or C0G dielectric capacitors are good choices for AC-coupling capacitors. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

Charge-Pump Flying Capacitor

The charge-pump flying capacitor connected between C1N and C1P affects the charge pump's load regulation and output impedance. Choosing a flying capacitor that is too small degrades the MAX9723's ability to provide sufficient current drive and leads to a loss of output voltage. Increasing the value of the flying capacitor improves load regulation and reduces the charge-pump output impedance. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*.

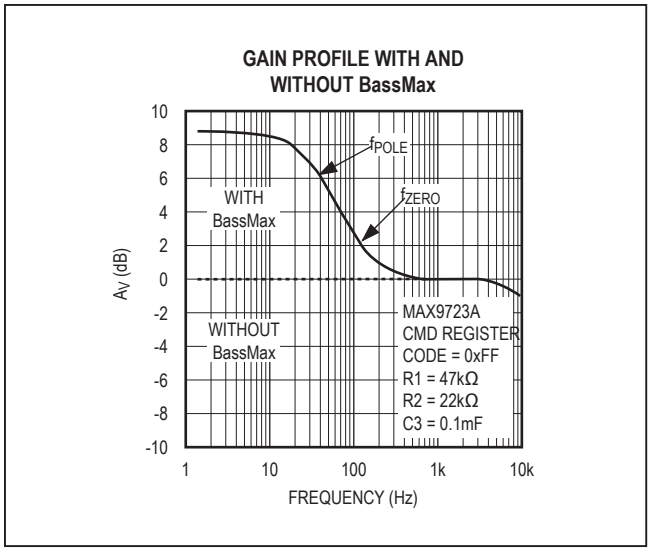


Figure 11. BassMax, Gain Profile Example

Charge-Pump Hold Capacitor

The hold capacitor's value and ESR directly affect the ripple at PV_{SS}. Ripple is reduced by increasing the value of the hold capacitor. Choosing a capacitor with lower ESR reduces ripple and output impedance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Charge-Pump Capacitance and Load Resistance graph in the *Typical Operating Characteristics*.

BassMax Gain-Setting Components

The bass-boost low-frequency response, when BassMax is enabled, is set by the ratio of R1 to R2 by the following equation (see Figure 2):

$$A_{V_BOOST} = 20 \times \log\frac{R1+R2}{R1-R2}$$

where A_{V_BOOST} is the voltage gain boost in dB at low frequencies. A_{V_BOOST} is added to the gain realized by the volume setting. The absolute gain at low frequencies is equal to:

$$A_{V_TOTAL} = A_{V_VOL} + A_{V_BOOST}$$

where A_{V_VOL} is the gain due to the volume setting, and A_{V_TOTAL} is the absolute gain at low frequencies. To maintain circuit stability, the ratio:

$$R2/(R1 + R2)$$

must not exceed 1/2. A ratio equaling 1/3 is recommended. The switch that shorts BB_ to SGND, when BassMax is disabled, can have an on-resistance as high as 300Ω. Choose a value for R1 that is greater than 40kΩ to ensure that positive feedback is negligible when BassMax is disabled. Table 12 contains a list of R2 values, with R1 = 47kΩ, and the corresponding low-frequency gain.

The low-frequency boost attained by the BassMax circuit is added to the gain realized by the volume setting. Select the BassMax gain so that the output signal will remain within the dynamic range of the MAX9723. Output signal clipping will occur at low frequencies if the BassMax gain boost is excessively large (see the *Output Dynamic Range* section).

Capacitor C3 forms a pole and a zero according to the following equations:

$$f_{POLE} = \frac{R1-R2}{2\pi \times C3 \times R1 \times R2}$$

$$f_{ZERO} = \frac{R1+R2}{2\pi \times C3 \times R1 \times R2}$$

f_{POLE} is the frequency at which the gain boost begins to roll off. f_{ZERO} is the frequency at which the bass-boost gain no longer affects the transfer function and the volume-control gain dominates. Table 13 contains a list of capacitor values and the corresponding poles and zeros for a given DC gain. See Figure 11 for an example of a gain profile using BassMax.

Custom Maximum Gain Setting Using BassMax

The circuit in Figure 12 uses the BassMax function to increase the maximum gain of the MAX9723. The gain boost created with the circuit in Figure 12 is added to the maximum gain selected by Bit 5 in the command register. Set the maximum gain with RA and RB using the following equation:

$$A_{V_TOTAL} = A_{V_VOL} + 20 \times \log\left(\frac{RA+RB}{RA-RB}\right)$$

where A_{V_VOL} is the gain due to the volume setting, and A_{V_TOTAL} is the absolute passband gain in dB.

Capacitor CA blocks any DC offset from being gained, but allows higher frequencies to pass. CA creates a pole that indicates the low-frequency point of the pass band. Choose CA so that the lowest frequencies of interest are not attenuated. For a typical application, set f_{POLE} equal to or below 20Hz.

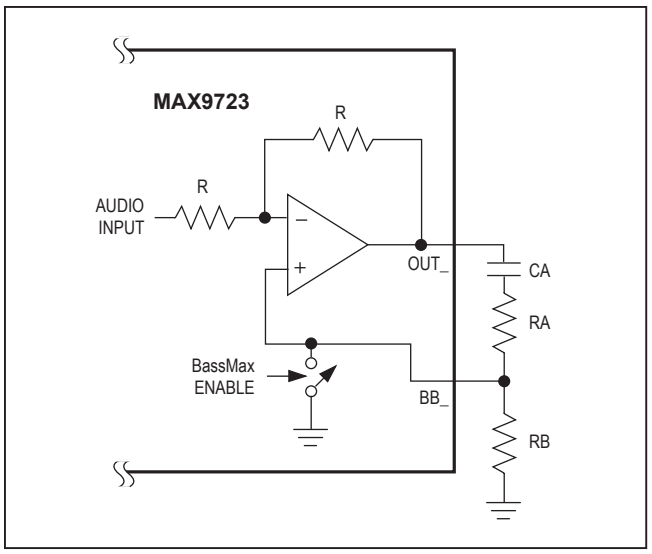


Figure 12. Using BassMax to Increase MAX9723's Maximum Gain

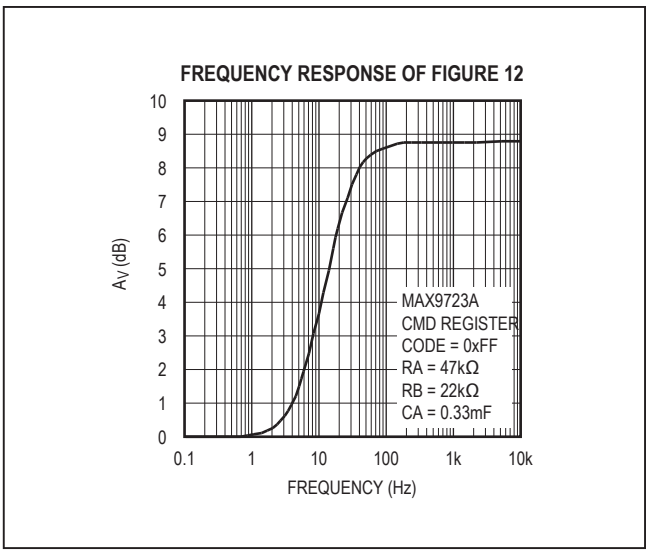


Figure 13. Increasing the Maximum Gain Using BassMax

Table 12. BassMax Gain Examples (R1 = 47kΩ)

R2 (kΩ)	A_V GAIN (dB)
39	20.6
33	15.1
27	11.3
22	8.8
15	5.7
10	3.7

Table 13. BassMax Pole and Zero Examples for a Gain Boost of 8.8dB (R1 = 47kΩ, R2 = 22kΩ)

C3 (nF)	f_{POLE} (Hz)	f_{ZERO} (Hz)
100	38	106
82	47	130
68	56	156
56	68	190
47	81	230
22	174	490
10	384	1060

$$CA = \frac{1}{2\pi f_{POLE} \times (RA - RB)}$$

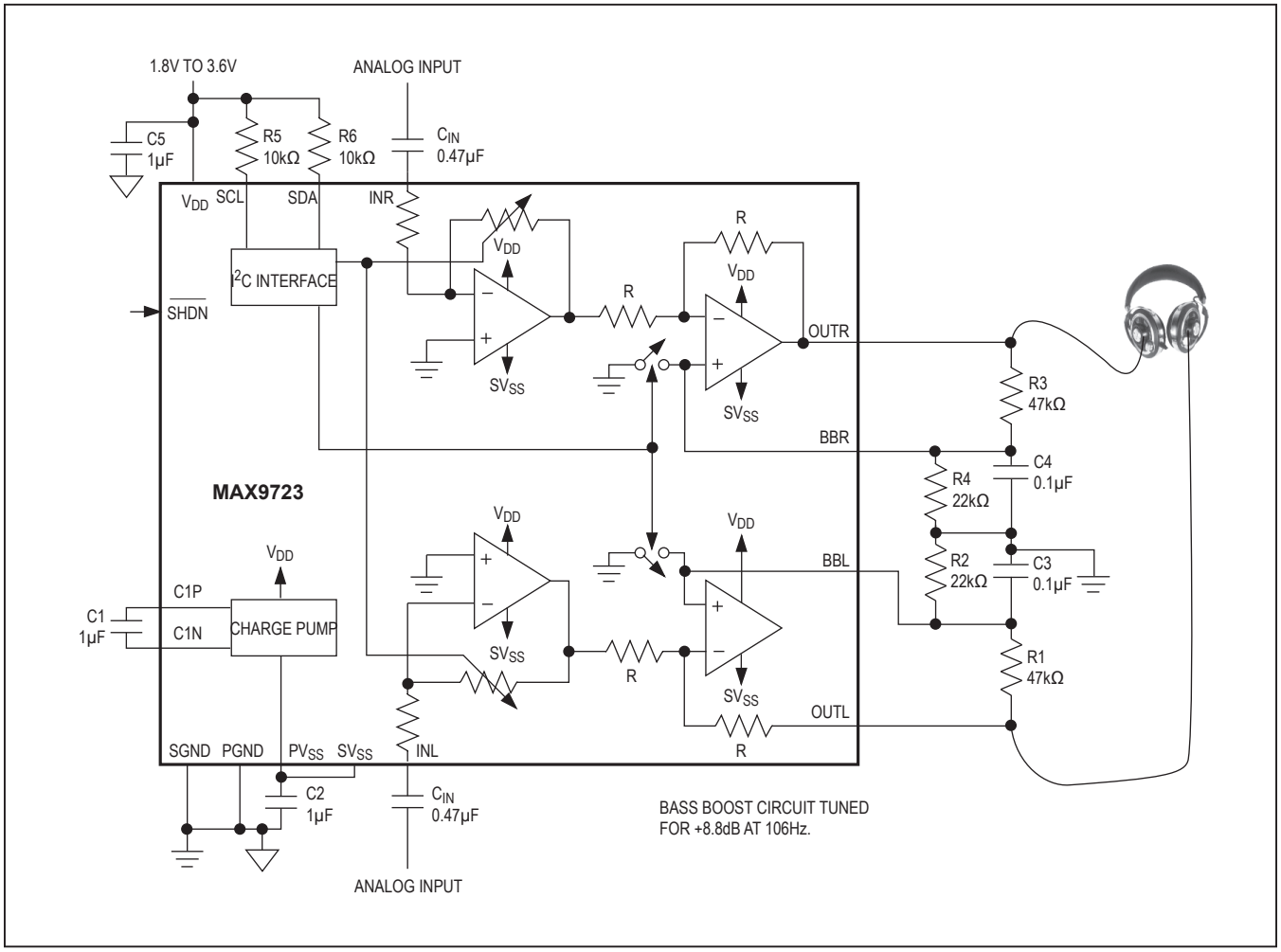
Figure 13 shows the frequency response of the circuit in Figure 12. With RA = 47kΩ, RB = 22kΩ, and CA = 0.33µF, the passband gain is set to 8.8dB.

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Connect PGND and SGND together at a single point on the PC board. Connect PV_{SS} to SV_{SS} and bypass with a 1µF capacitor to PGND. Bypass V_{DD} to PGND with a 1µF capacitor. Place the power-supply bypass capacitor and the charge-pump capacitors as close to the MAX9723 as possible. Route PGND and all traces that carry switching transients away from SGND and the audio signal path. Route digital signal traces away from the audio signal path. Make traces perpendicular to each other when routing digital signals over or under audio signals.

The thin QFN package features an exposed paddle that improves thermal efficiency. **Ensure that the exposed paddle is electrically isolated from PGND, SGND, and V_{DD}. Connect the exposed paddle to SV_{SS} when the board layout dictates that the exposed paddle cannot be left floating.**

Functional Diagram/Typical Operating Circuit



UCSP Applications Information

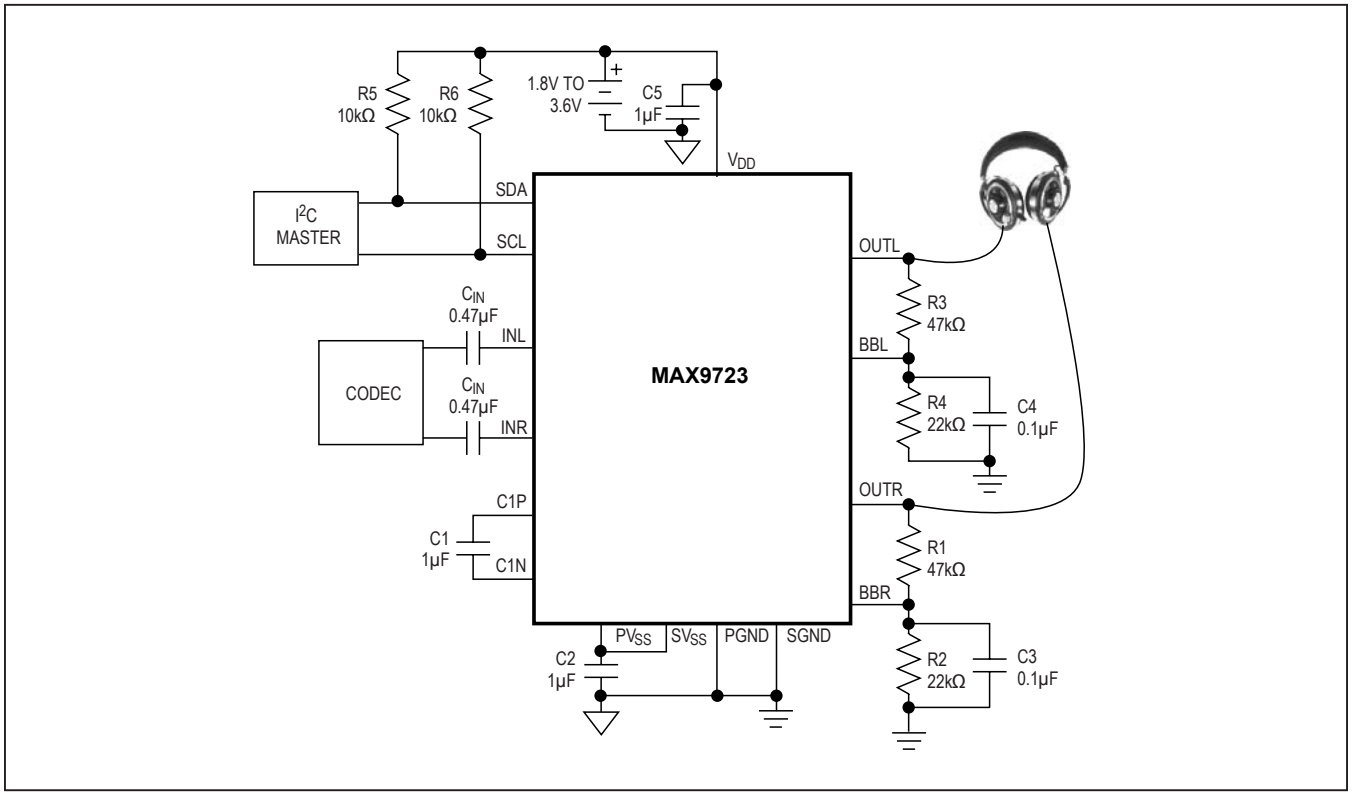
For the latest application details on UCSP construction, dimensions, tape carrier information, PC board techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, go to Maxim's website at **www.maximintegrated.com/ucsp** and look up Application Note 1891: Understanding the Basics of the Wafer-Level Chip-Scale Package (WL-CSP).

Chip Information

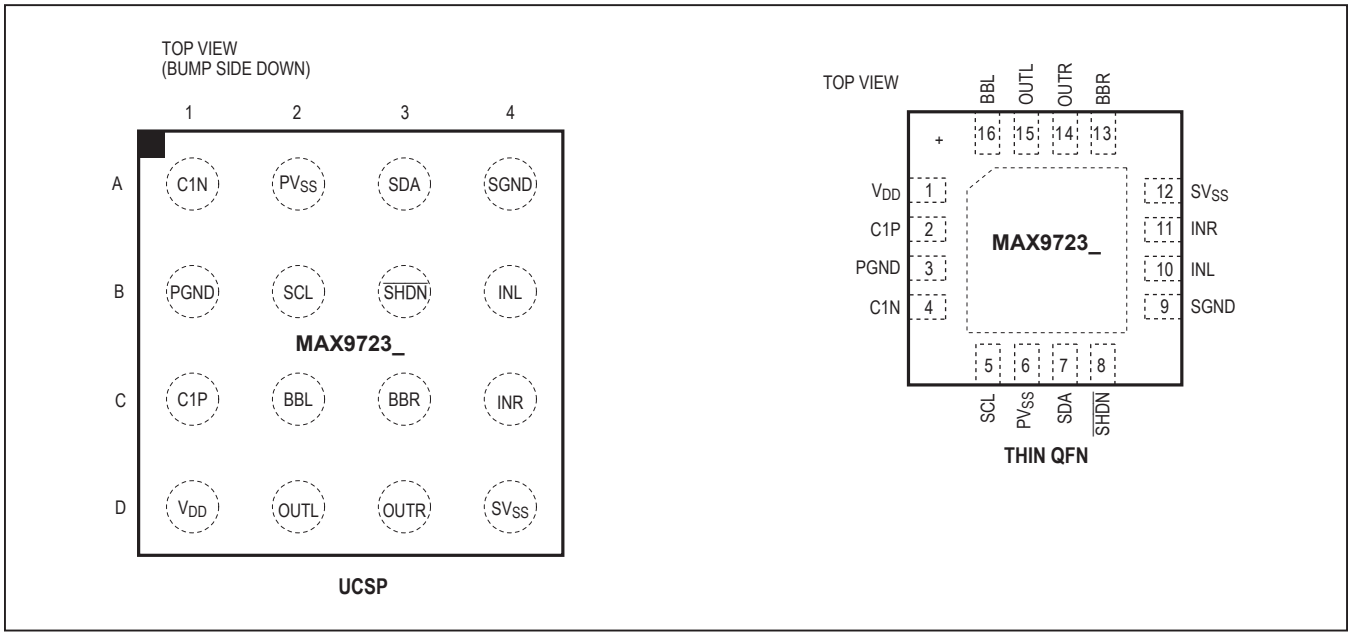
TRANSISTOR COUNT: 7165

PROCESS: BiCMOS

System Diagram



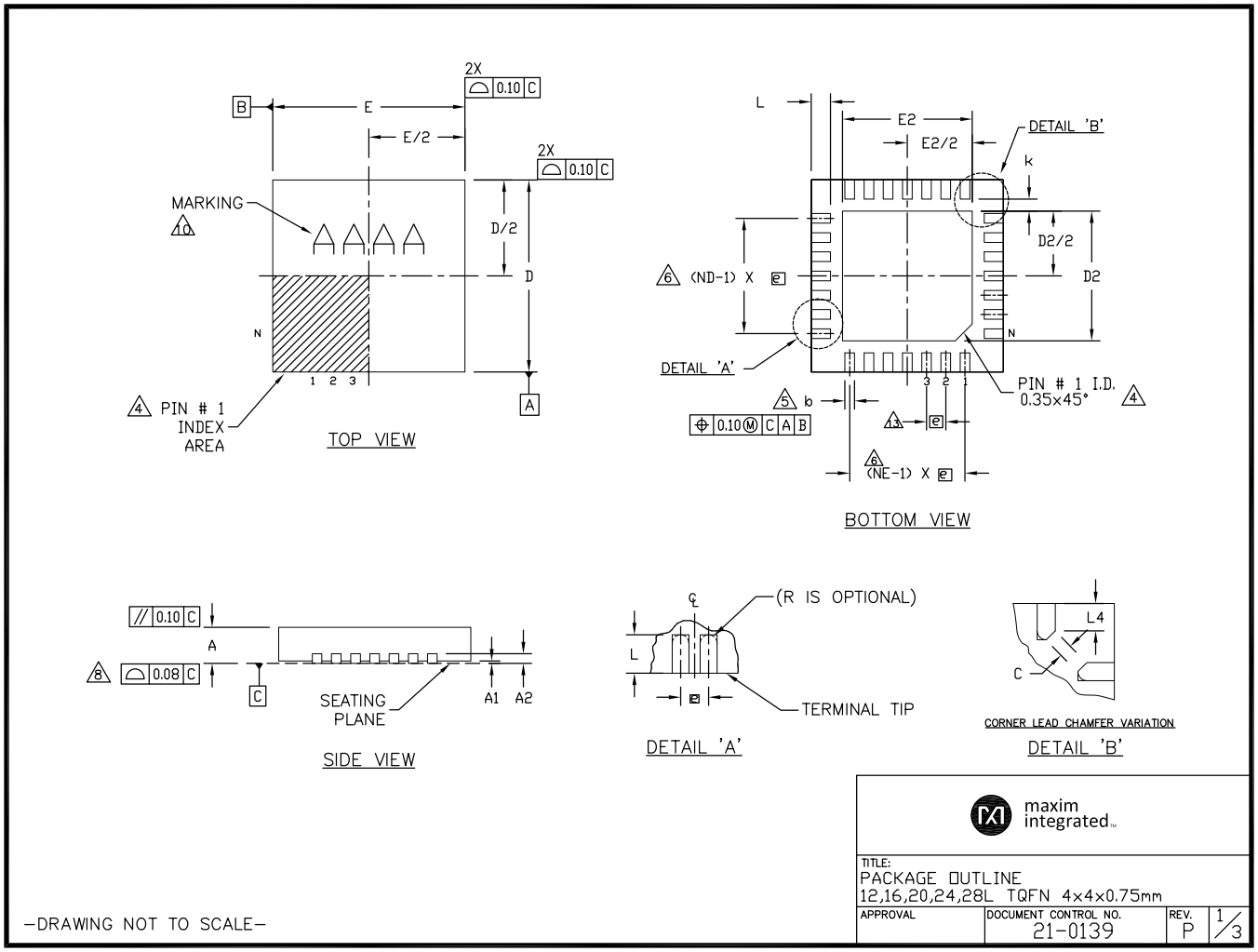
Pin Configurations



Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1644-4	**21-0139**	**90-0070**
16 UCSP	B16-1	**21-0101**	Refer to **Application Note 1891**



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

DIMENSION VARIATIONS

PKG. CODE	D2			E2			L			R (LEAD TIP RADIUS)
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T2044-4	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35	0.125 REF
T2044-4C	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35	0.125 REF
T2044-5	2.60	2.70	2.80	2.60	2.70	2.80	0.35	0.40	0.45	0.203 REF

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4C	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-3C	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4C	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444MK-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70
T2844-1C	2.50	2.60	2.70	2.50	2.60	2.70
T2844N-1	2.65	2.70	2.75	2.65	2.70	2.75

CORNER LEAD CHAMFER VARIATION

PKG. CODES	C	L4
T2444-2	0.120 X 45° REF	0.31 REF
T2444-3	0.120 X 45° REF	0.31 REF
T2444-3C	0.120 X 45° REF	0.31 REF
T2444-4	0.120 X 45° REF	0.31 REF
T2444-4C	0.120 X 45° REF	0.31 REF
T2444M-1	0.120 X 45° REF	0.31 REF
T2444MK-1	0.120 X 45° REF	0.31 REF
T2444N-4	0.120 X 45° REF	0.31 REF

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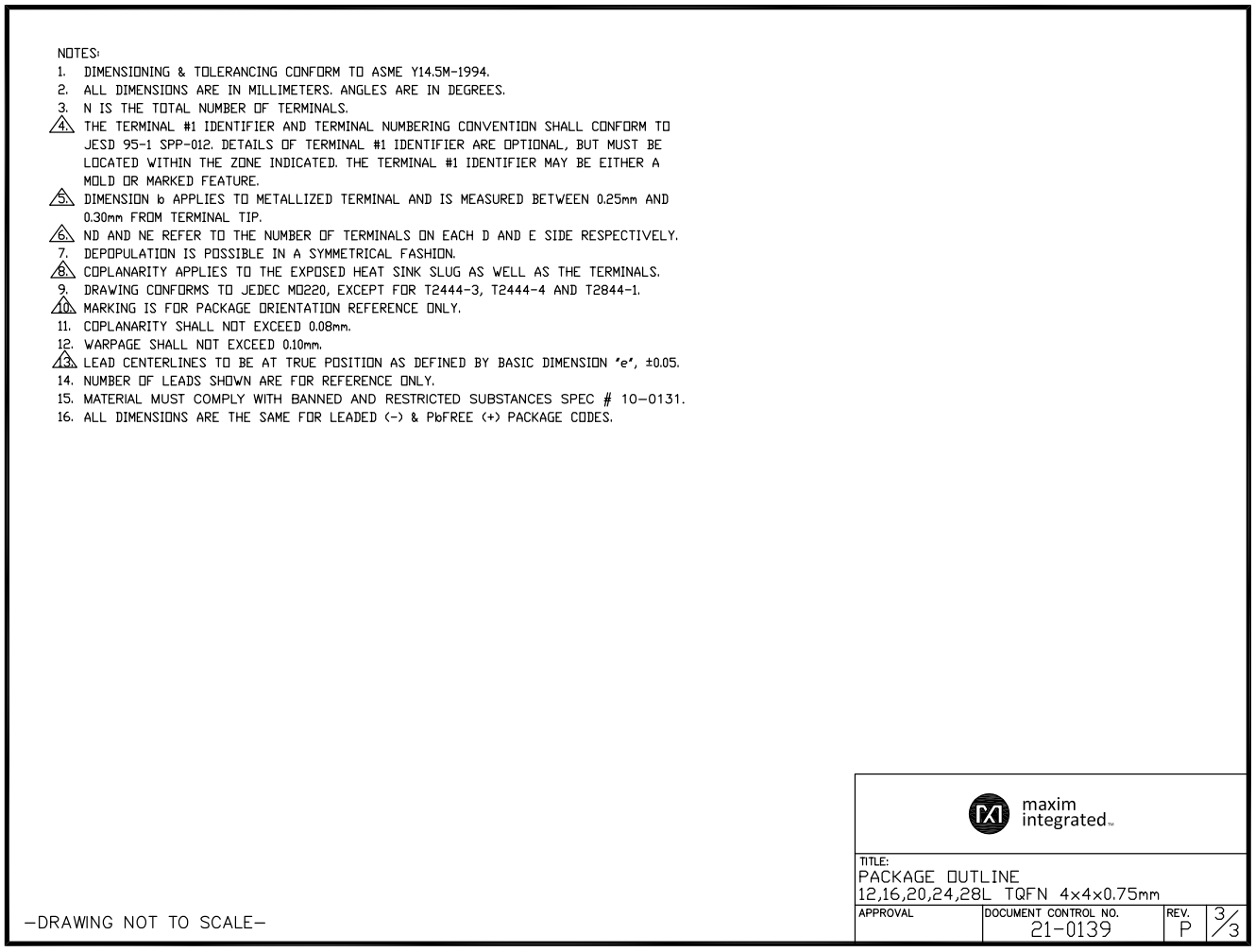
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PACKAGE OUTLINE
12,16,20,24,28L TQFN 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	P	2/3

–DRAWING NOT TO SCALE–

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
16. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

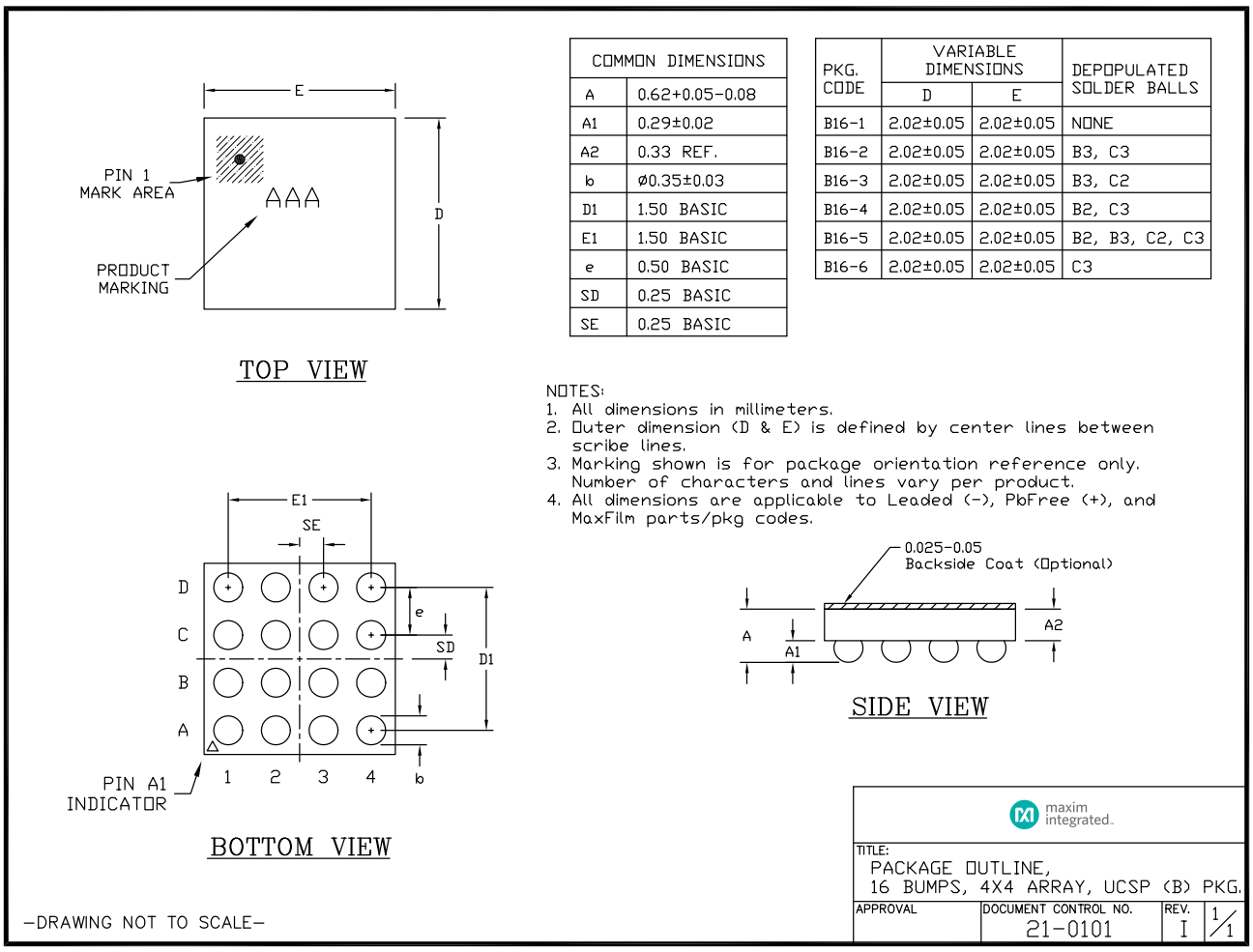
maxim integrated

TITLE:
PACKAGE OUTLINE
12,16,20,24,28L TQFN 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	P	3/3

Package Information (continued)

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COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B16-1	2.02±0.05	2.02±0.05	NONE
B16-2	2.02±0.05	2.02±0.05	B3, C3
B16-3	2.02±0.05	2.02±0.05	B3, C2
B16-4	2.02±0.05	2.02±0.05	B2, C3
B16-5	2.02±0.05	2.02±0.05	B2, B3, C2, C3
B16-6	2.02±0.05	2.02±0.05	C3

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	8/08	Updated TQFN pin configuration, and corrected *Typical Operating Circuit* and *System Diagram* pin names	20, 21
3	7/14	Removed automotive reference in *Applications* section	1
4	7/14	Updated Table 8, Table 10, and replaced Figures 7 through 10	15, 16, 17

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